CLAIMS

1. A computer network comprising: - a plurality of processing nodes, at least two of which each having respective addressable memories and respective network interfaces; and a switching network which operatively connects the plurality of processing nodes together, each network interface including a memory management unit having associated with it a memory in which is stored (a) at least one mapping table for mapping 64 bit virtual addresses to the physical addresses of the addressable memory of the respective processing node; and (b) instructions for applying a compression algorithm to said virtual addresses, the at least one mapping table comprising a plurality of virtual addresses and their associated physical addresses ordered with respect to compressed versions of the 64 bit virtual addresses.

2. A computer network as claimed in claim 1, wherein the memory management unit of the network interface includes two translation lookaside buffers.

3. A computer network as claimed in claim 2, further comprising a thread processor and a microcode processor, wherein one translation lookaside buffer of the memory management unit is dedicated to the thread processor and the other translation lookaside buffer is dedicated to the microcode processor of the network interface.

4. A computer network as claimed in claim 1, wherein each entry of the mapping table of the memory management unit includes two tags representative of two virtual addresses.

5. A computer network as claimed in claim 4, wherein each tag is associated with four physical memory addresses.

6. A computer network as claimed in claim 1, wherein each entry of the mapping table further includes a chain pointer, which is used to identify alternate entries in the mapping table for different virtual addresses having identical compressed virtual addresses.

7. A method of reading or writing to a memory area of the addressable memory of a processor in a computer network, comprising the steps of:

inputting a memory access command to a network interface associated with the processor, the network interface having a memory management unit in which is stored at least one mapping table mapping 64 bit virtual addresses to the physical addresses of the addressable memory of the processor, the contents of the mapping table being ordered with respect to compressed versions of the 64 bit virtual addresses;

compressing the virtual address of the memory access for which a corresponding physical address is required;

locating a mapping table entry in the mapping table of the network interface on the basis of the compressed version of the virtual address;

comparing the virtual address of the located mapping table entry with the virtual address for which a corresponding physical address is required;

where the comparison confirms the virtual address of the located mapping table entry matches the virtual address of the memory access command, reading one or more physical addresses associated with the matched virtual address; and

the network interface actioning the memory access command.

8. A method as claimed in claim 7, including the additional step of before compressing the virtual address, comparing the 64 bit virtual address for which a corresponding physical address is required with 64 bit virtual addresses stored in one or more lookaside buffers and where a

match is found, reading the one or more physical addresses associated with the matched virtual address stored in the lookaside buffer.

9. A method as claimed in claim 7, wherein the memory management unit of the network interface supports two separate page sizes with separate mapping tables for each page size and wherein the content of each mapping table is search in turn to locate an entry relevant to the virtual address of the memory access.

10. A network interface adapted to operatively connect to a network of processing nodes a respective processing node having an associated addressable memory, the network interface including a memory management unit having associated with it a memory in which is stored the following: - (a) at least one mapping table for mapping 64 bit virtual addresses to the physical addresses of the addressable memory of the respective processing node; and (b) instructions for applying a compression algorithm to said virtual addresses, the at least one mapping table comprising a plurality of virtual addresses and their associated physical addresses ordered with respect to compressed versions of the 64 bit virtual addresses.

11. A network interface as claimed in claim 10, wherein the memory management unit of the network interface includes two translation lookaside buffers.

12. A network interface as claimed in claim 11, further comprising a thread processor and a microcode processor, wherein one translation lookaside buffer of the memory management unit is dedicated to the thread processor and the other translation lookaside buffer is dedicated to the microcode processor of the network interface.

13. A network interface as claimed in claim 10, wherein each entry of the mapping table of the memory management unit includes two tags representative of two virtual addresses.

14. A network interface as claimed in claim 13, wherein each tag is associated with four physical memory addresses.

15. A network interface as claimed in claim 10, wherein each entry of the mapping table further comprises a chain pointer, which is used to identify alternate entries in the mapping table for different virtual addresses having identical compressed virtual addresses.